Remarks

Applicant and his representatives wish to thank Examiner Thomas for the thorough examination of the present application, the detailed explanations in the Office Action dated February 13, 2004, and the indication that Claim 4 (if rewritten to overcome rejections under 35 USC 112, second paragraph and to include all of the limitations of Claim 2) is allowable. New Claim 11 generally corresponds to the allowable Claim 4 in the above Amendment. While not all of the explicit limitations of original Claim 2 have been retained in the above Amendment, the amendments to Claim 2 are not believed to affect the reasons for allowability given in the Office Action dated February 13, 2004.

The present invention relates to a method for fabricating MOS transistors that is capable of reducing junction capacitance without degrading transistor characteristics, even in narrow gate width transistors. The method (as set forth in amended Claim 1 above) generally comprises the steps of:

a) forming a buffer oxide layer on a semiconductor substrate having an isolation layer;
b) conducting ion implantations for well formation and field stop formation through the buffer oxide layer;
c) removing the buffer oxide layer;
d) forming a sacrificial layer on the semiconductor substrate;
e) patterning the sacrificial layer to form a trench defining a gate electrode forming region; and
f) conducting ion implantations for threshold voltage adjustment and punch stop formation in the semiconductor substrate area under the trench.

The method set forth in new Claim 20 above generally comprises:

a) conducting ion implantations for threshold voltage adjustment and punch stop formation in a semiconductor substrate area exposed in a trench in a patterned sacrificial oxide layer on the substrate;

b) forming a gate electrode in the trench;

c) removing the patterned sacrificial oxide layer; and

d) forming LDD regions, side wall spacers, and source/drain regions.

The references cited against the originally-filed claims (Shao et al, U.S. Pat. No. 6,410,394 [hereinafter "Shao '394"], Stolmeijer et al., U.S. Pat. No. 5,384,279 [hereinafter "Stolmeijer"], and Squillace et al., U.S. Pat. No. 3,859,222 [hereinafter "Squillace"]) neither disclose nor suggest removing a buffer oxide layer before conducting ion implantation for punch stop formation (amended Claims 1 and 2). Furthermore, the cited references neither disclose nor suggest conducting ion implantations for threshold voltage adjustment and punch stop formation in a semiconductor substrate area exposed in a trench in a patterned sacrificial oxide layer (new Claim 20). Consequently, the present claims are patentable over the cited references.

The Rejection of Claims 1, 7 and 8 under 35 U.S.C. § 102

The rejection of Claims 1, 7 and 8 under 35 U.S.C. § 102 as being anticipated by Stolmeijer is respectfully traversed.

Stolmeijer discloses a method of manufacturing a semiconductor device, comprising a silicon body (1) having a surface (4) where there are situated a number of semiconductor regions (5, 6) and field oxide regions (7) (Abstract, ll. 1-4). After the field oxide regions have been provided, the semiconductor regions are formed by implantations of n-type and p-type dopants (Abstract, ll. 4-7). Stolmeijer discloses the formation of semiconductor regions 5, 6 by combining each n-type dopant implantation with a p-type dopant implantation (col. 6, ll. 25-31). The semiconductor region 5 is formed with an n-well implantation 10 and an anti-punch-through implantation 11, and the semiconductor region 6 is formed with a p-well implantation 12 and an anti-punch-through implantation 13 (col. 7, ll. 26-31).

The implantations 10, 11, 12, 13 and 14 were performed through a layer of silicon oxide 16 having a thickness of approximately 25 nm (col. 7, ll. 49-52). After the implantations, Stolmeijer discloses removing the layer of silicon oxide 16 and replacing it with a layer of gate

oxide 17 having a thickness of approximately 15 nm (col. 7, ll. 52-54). Thus, Stolmeijer does not disclose or suggest removing silicon oxide layer 16 before conducting ion implantation for punch stop formation. Arguably, silicon oxide layer 16 corresponds to the presently claimed buffer oxide, because ion implantations for well formation are conducted through it (col. 7, ll. 1-31, and col. 8, ll. 49-52), and it is removed before forming gate oxide layer 17, lightly doped zones 21 and strongly doped zones 22 and 24 (the latter two of which appear to correspond to LDD regions and transistor source/drain regions, respectively; see, e.g., col. 8, ll. 52-54; col. 9, ll. 43-64; and FIGS. 4-5).

Furthermore, Stolmeijer is silent with regard to (i) patterning a layer to form a trench defining a gate electrode forming region and (ii) conducting ion implantations for threshold voltage adjustment and punch stop formation through such a trench (amended Claims 1 and 2). Stolmeijer is silent with regard to conducting ion implantations for threshold voltage adjustment and punch stop formation in a semiconductor substrate area exposed in a trench in a patterned sacrificial oxide layer (new Claim 20). Therefore, this ground of rejection is unsustainable, and should be withdrawn.

The Rejection of Claims 2, 3, 5, 7 and 8 under 35 U.S.C. § 103

The rejection of Claims 2, 3, 5, 7 and 8 under 35 U.S.C. § 103 as being unpatentable over Shao '394 in view of Stolmeijer is respectfully traversed.

Claim 2, as amended, generally recites the same or substantially similar limitations as amended Claim 1 above. Thus, for essentially the same reasons as for amended Claim 1, amended Claim 2 is patentable over the cited references.

Shao '394 discloses a method for forming a CMOS transistor gate with a self-aligned channel implant (Abstract, ll. 1-2). After well formation (col. 3, ll. 26-28 and FIG. 1A), a first insulating layer (20), preferably composed of silicon dioxide having a thickness of between about 50 Angstroms and 400 Angstroms, is formed on the semiconductor structure (11) (col. 3, ll. 34-38). A second insulating layer (30), preferably composed of silicon nitride having a

thickness of between about 2000 Angstroms and 4000 Angstroms, is formed on the first insulating layer (20) (col. 3, ll. 39-43). The second insulating layer (30) is patterned to form a first channel implant opening (35) for an NMOS gate and a second channel implant opening (37) for a PMOS gate, using a poly reverse mask (32) (col. 3, ll. 46-49). Two implant steps are performed through the exposed channel implant openings (35) and (37), a first implant to form threshold voltage adjust regions (39) and (41), and a second implant to form anti-punchthrough regions (36) and (38) (col. 4, ll. 10-40).

Shao '394 then discloses forming a gate layer on first insulating layer (20), over the areas of the semiconductor substrate (11) corresponding to the n-well and p-well active regions (see col. 3, ll. 10-12; col. 4, ll. 57-59; and FIGS. 1A and 3). The gate layer completely fills the channel implant openings, then is planarized to form first and second gate electrodes (40) and (50) using CMP (col. 4, ll. 61-67). The second insulating layer (30) is then removed, preferably using an etch selective to the first insulating layer (20) and the first and second gate electrodes (40, 50) (col. 5, ll. 1-4). Thereafter, source and drain structures, including LDD regions, are formed, apparently and/or presumably through the first insulating layer (20) (col. 5, ll. 9-30, and FIG. 4).

Shao '394 is silent with regard to removing first insulating layer (20), which arguably corresponds to the present buffer oxide (Claims 1 and 2). (No part of the first insulating layer (20) of Shao '394 is not removed or patterned, and therefore, cannot correspond to the sacrificial layer of the present Claims 1-2 or the patterned sacrificial oxide layer of the present Claim 20.) Thus, Shao '394 cannot disclose or suggest removing a buffer oxide layer before conducting ion implantations for threshold voltage adjustment and punch stop formation, as is recited in amended Claims 1 and 2.

Furthermore, Shao '394 is silent with regard to a patterned sacrificial oxide layer through which ion implantations for threshold voltage adjustment and punch stop formation are conducted (new Claim 20). The second insulating layer (30) of Shao '394 is patterned to form channel implant openings and is subsequently removed. Thus, the second insulating layer (30) of Shao '394 arguably corresponds to the present patterned sacrificial oxide layer in new Claim

20. However, as the Examiner correctly recognized, Shao '394 appears to teach away from an sacrificial layer composed of oxide (see the paragraph bridging pages 10-11 of the Office Action dated February 13, 2004). Thus, Shao '394 cannot disclose or suggest conducting ion implantations for threshold voltage adjustment and punch stop formation through a trench in a patterned sacrificial oxide layer, as recited in new Claim 20.

Stolmeijer fails to cure the salient deficiencies of Shao '394. As discussed above, Stolmeijer discloses conducting anti-punch-through implantations 11 and 13 through a layer of silicon oxide 16 (col. 7, ll. 26-52). As discussed above, silicon oxide layer 16 arguably corresponds to the presently claimed buffer oxide, because (1) ion implantations for well formation are conducted through it, and (2) it is removed before forming gate oxide layer 17, lightly doped zones 21 and strongly doped zones 22 and 24. The silicon oxide layer 16 of Stolmeijer does not correspond to the sacrificial layer recited in amended Claims 1 and 2, because silicon oxide layer 16 is not patterned, it is not removed before conducting ion implantation for punch stop formation, and Stolmeijer does not disclose removal of a different oxide layer prior to its formation.

Stolmeijer also discloses a gate oxide layer 17, which arguably corresponds to the sacrificial layer recited in amended Claims 1 and 2, since it is formed after removal of silicon oxide layer 16 (col. 8, ll. 52-54). However, in this case, Stolmeijer is silent with regard to patterning gate oxide layer 17 to form a trench through which one conducts ion implantations for threshold voltage adjustment and punch stop formation, as is recited in amended Claims 1 and 2. As discussed above, Stolmeijer discloses ion implantations for punch stop formation only through silicon oxide layer 16. Also, Stolmeijer discloses ion implantations for threshold voltage adjustment only through unpatterned gate oxide layer 17 (see, e.g., col. 7, ll. 26-52; col. 8, ll. 57-68; col. 9, ll. 1-2; and FIG. 3). Thus, Stolmeijer fails to cure the salient deficiencies of Shao '394 with regard to (i) removing a buffer oxide layer before conducting ion implantation for punch stop formation, as is recited in amended Claims 1 and 2, and/or (ii) conducting ion implantations for threshold voltage adjustment and punch stop formation through a trench in a patterned sacrificial oxide layer, as recited in new Claim 20.

As a result, neither reference, alone or in combination, discloses or suggests (i) removing a buffer oxide layer before conducting ion implantation for punch stop formation and/or (ii) conducting ion implantation for threshold voltage adjustment through a trench in a patterned sacrificial oxide layer, as is recited in amended Claims 1 and 2 and new Claim 20. Consequently, this ground of rejection is unsustainable, and should be withdrawn.

The Rejection of Claim 6 under 35 U.S.C. § 103

The rejection of Claim 6 under 35 U.S.C. § 103 as being unpatentable over Shao '394 in view of Stolmeijer and Squillace is respectfully traversed.

Claim 6, which includes all of the limitations as amended Claim 1 above, further recites that patterning of the sacrificial layer comprises wet-etching the sacrificial layer. Applicants' undersigned representative does not dispute that Squillace discloses a process for wet etching silicon nitride-silicon oxide composite structures (col. 1, ll. 7-10). However, Squillace is silent with regard to (i) removing a buffer oxide layer before conducting ion implantation for punch stop formation, as is recited in amended Claims 1 and 2, and/or (ii) conducting ion implantation for threshold voltage adjustment through a trench in a patterned sacrificial layer, as is recited in amended Claims 1 and 2 and new Claim 20. Thus, Squillace cannot cure the salient deficiencies of Shao '394 and Stolmeijer regarding these claimed steps, and for essentially the same reasons as amended Claims 1 and 2 and new Claim 20, Claim 6 is patentable over the cited references. Nonetheless, Claim 6 and similar new Claim 13 are independently patentable over the cited references, as will be explained below.

More specifically, the wet-etching method of Squillace utilizes a phosphoric acid-fluoboric acid mixture (col. 2, ll. 9-10; also see col. 3, ll. 1-28). However, there is no indication in either Squillace or Shao '394 that the wet etching process of Squillace is equivalent to or interchangeable with the dry etching method of Shao '394. In fact, the references themselves clearly indicate that the two processes are not interchangeable, largely for a reason recognized by the Examiner in the Office Action of February 13, 2004.

The Examiner noted that Shao forms trenches in a sacrificial layer using an etchant having a high selectivity for etching the sacrificial layer, relative to the gate insulating layer (see p. 11, ll. 1-3 of the Office Action dated February 13, 2004). Thus, the dry etching method of Shao '394 was chosen because it preferentially etches silicon nitride (the preferred sacrificial layer material of Shao '394) over silicon oxide (the preferred gate insulating layer material of Shao '394). However, quite to the contrary, the wet etching process of Squillace is carefully designed to etch silicon nitride and silicon oxide at the same rate (see col. 3, ll. 13-20, and col. 4, ll. 15-17). Thus, rather than suggesting that the etching processes disclosed therein may be interchangeable, the Squillace and Shao '394 references clearly teach that they are not interchangeable, because one would get completely different selectivity results if one did, in fact, attempt to substitute one process for the other.

Consequently, one of ordinary skill in the art would not substitute the wet-etching method of Squillace for the dry etching method of Shao '394. As a result, Claims 6 and 13 are independently patentable over the cited references.

The Rejections of Claim 3 under 35 U.S.C. § 112, First Paragraph, and of Claims 2-8 under 35 U.S.C. § 112, Second Paragraph

The rejections of Claim 3 under 35 U.S.C. § 112, first paragraph, and of Claims 2-8 under 35 U.S.C. § 112, second paragraph have been obviated by appropriate amendment.

The Objections to the Drawings, the Specification, the Abstract, and Claim 2

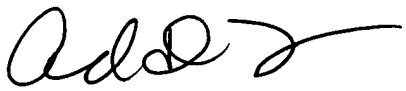
The objections to the drawings, the specification, the Abstract, and Claim 2 have all been overcome by appropriate amendment.

Conclusions

In view of the above amendments and remarks, all bases for objection and rejection are believed to be overcome, and the application is believed to be in condition for allowance. Early notice to that effect is earnestly requested.

If it is deemed helpful or beneficial to the efficient prosecution of the present application, the Examiner is invited to contact Applicant's undersigned representative by telephone.

Respectfully submitted,



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